CLAIMS:

1. A semiconductor storage device comprising:

a semiconductor substrate (1, 111, 187);

a gate insulating film (12, 114) formed on the semiconductor substrate (1, 111, 187);

a single gate electrode (13, 117) formed on the gate insulating film (12, 114);

two charge holding portions (61, 62, 161, 162, 162a) formed on the sidewalls on opposite sides of the single gate electrode (13, 117);

two diffusion layer regions (17, 18, 112, 113) corresponding to the two charge holding portions (61, 62, 161, 162, 162a), respectively; and

a channel region placed beneath the single gate electrode (13, 117), wherein

the charge holding portions (61, 62, 161, 162, 162a) have a structure such that a film made of a first insulator (15, 142, 142a) having a function of holding charge is sandwiched between a second insulator (14, 141, 141a) and a third insulator (16, 143), and

the charge holding portions (61, 62, 161, 162, 162a) are constituted such that the amount of current flowing between one of the diffusion layer regions (17, 18, 112, 113) and the other of the diffusion layer regions (17, 18, 112, 113) at the time of application of a voltage to

the gate electrode (13, 117) is changed due to the quantity of charge held in the first insulator (15, 142, 142a).

2. The semiconductor storage device according to Claim 1, wherein expressions $\chi1 > \chi2$ and $\chi1 > \chi3$ are satisfied, where

the $\chi1$ represents an energy gap between the vacuum level and the lowest level of a conduction band of the first insulator (15, 142, 142a),

the $\chi2$ represents an energy gap between the vacuum level and the lowest level of a conduction band of the second insulator (14, 141, 141a), and

the $\chi3$ represents an energy gap between the vacuum level and the lowest level of a conduction band of the third insulator (16, 143).

3. The semiconductor storage device according to Claim 1, wherein expressions $\Phi1 < \Phi2$ and $\Phi1 < \Phi3$ are satisfied, where

the $\Phi1$ represents an energy gap between the vacuum level and the highest level of a valence band of the first insulator (15, 142, 142a),

the $\Phi2$ represents an energy gap between the vacuum level and the highest level of a valence band of the second insulator (14, 141, 141a), and

the $\Phi 3$ represents an energy gap between the vacuum level and the highest level of a valence band of the third insulator (16, 143).

4. The semiconductor storage device according to Claim 1, wherein all expressions of: $\chi 1 > \chi 2$, $\chi 1 > \chi 3$, $\Phi 1 < \Phi 2$ and $\Phi 1 < \Phi 3$ are satisfied, where

the $\chi 1$ represents an energy gap between the vacuum level and the lowest level of the conduction band of the first insulator (15, 142, 142a),

the $\chi 2$ represents an energy gap between the vacuum level and the lowest level of the conduction band of the second insulator (14, 141, 141a),

the $\chi 3$ represents an energy gap between the vacuum level and the lowest level of the conduction band of the third insulator (16, 143),

the $\Phi 1$ represents an energy gap between the vacuum level and the highest level of the valence band of the first insulator (15, 142, 142a),

the $\Phi 2$ represents an energy gap between the vacuum level and the highest level of the valence band of the second insulator (14, 141, 141a), and

the $\Phi 3$ represents an energy gap between the vacuum level and the highest level of the valence band of the third insulator (16, 143).

5. The semiconductor storage device according to Claim 1, wherein

the first insulator (15, 142, 142a) is of silicon nitride, and

the second and third insulators (14, 16, 141, 141a, 143) are of silicon oxide.

6. The semiconductor storage device according to Claim 5, wherein

the second insulator (14, 141, 141a) that is of silicon oxide is in a film form and separates the semiconductor substrate (1, 111, 187) from the first insulator (15, 142, 142a), and

the film formed of the second insulator (14, 141, 141a) on the semiconductor substrate (1, 111, 187) has a thickness of no less than 1.5 nm and of no greater than 15 nm.

7. The semiconductor storage device according to Claim 5, wherein

the film formed of the first insulator (15, 142, 142a), which is of silicon nitride, on the semiconductor substrate (1, 111, 187) has a thickness of no less than 2 nm and of no greater than 15 nm.

8. The semiconductor storage device according to Claim 1, wherein

the second insulator (14, 141, 141a) is in a film form and separates the semiconductor substrate (1, 111, 187) and the sidewalls of the gate electrode (13, 117) from the first insulator (15, 142, 142a), and

the thickness of the film made of the second insulator (14, 141, 141a) in the vicinity of the sidewalls of the gate electrode (13, 117) is greater than the thickness of the film made of the second insulator (14, 141, 141a) on the semiconductor substrate (1, 111, 187).

9. The semiconductor storage device according to Claim 5, wherein

the thickness of the film made of the second insulator (14, 141, 141a) on the semiconductor substrate (1, 111, 187) is less than the thickness of the gate insulating film (12, 114) and is not less than 0.8 nm.

10. The semiconductor storage device according to Claim 5, wherein

the thickness of the film made of the second insulator (14, 141, 141a) on the semiconductor substrate

(1, 111, 187) is greater than the thickness of the gate insulating film (12, 114) and is not greater than 20 nm.

11. The semiconductor storage device according to Claim 1, wherein

at least a portion of the film made of the first insulator (15, 142, 142a) having a function of charge storage overlaps a portion of the diffusion layer regions (17, 18, 112, 113).

12. The semiconductor storage device according to Claim 1, wherein

the film made of the first insulator (15, 142, 142a) having a function of charge storage includes a portion having a surface approximately parallel to the surface of the gate insulating film (12, 114).

13. The semiconductor storage device according to Claim 12, wherein

the film made of the first insulator (15, 142, 142a) having a function of charge storage includes a portion that extends approximately parallel to sides of the gate electrode (13, 117).